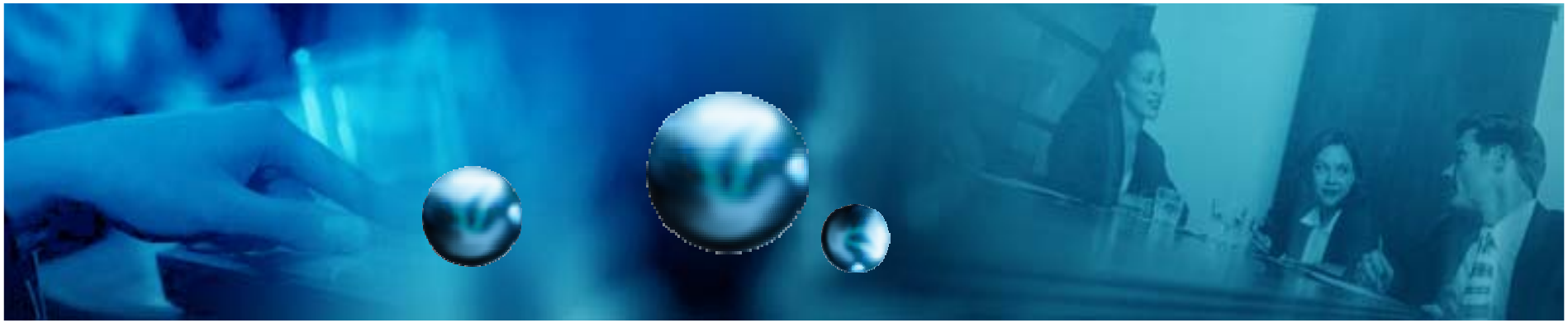

Full Adder Design

Design Practice - MyCAD

Table of Contents

- Preface
- XOR2 Design
  - XOR2 schematic and symbol
  - XOR2 simulation
  - XOR2 layout and results of verification
- AND2 Gate Design
  - AND2 gate schematic and symbol
  - AND2 simulation
  - AND2 gate layout and results of verification
- OR2 Gate Design
  - AND2 gate schematic and symbol
  - AND2 simulation
  - AND2 gate layout and results of verification
- Half Adder Design
  - Half Adder schematic and symbol
  - Half Adder simulation
  - Half Adder layout and results of verification
- Full Adder Design
  - Full Adder schematic and symbol
  - Full Adder simulation
  - Full Adder layout and results of verification

Preface

- This document provides the information on how to design Full Adder schematic and layout.
- Full Adder is designed based on MOSIS SCMOS layout rules.
- If you want to get more information, please refer to the related documents as below.
  - MyCAD Tutorial :
    Learn how to use schematic and layout editor.
  - MySpice Tutorial :
    Learn about simulating a circuit.
  - MyChip Pro Verification Reference Manual :
    Look up specific verification commands.

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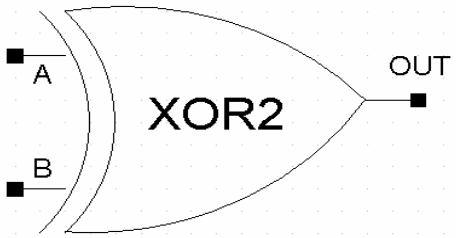
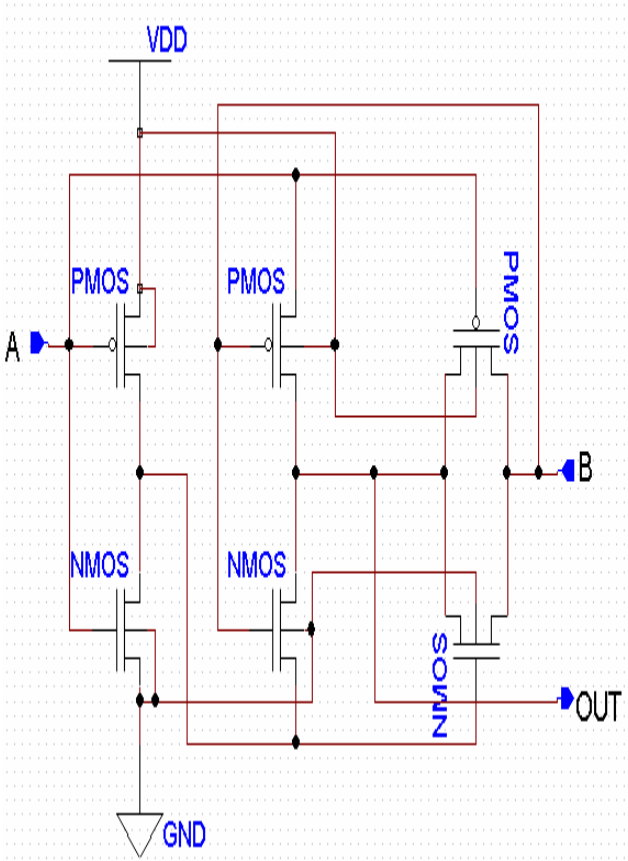
XOR2 schematic and symbol



Logic Symbol

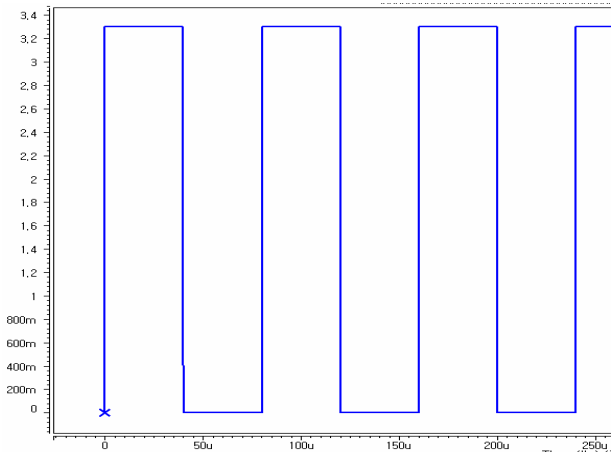
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

Truth Table



Schematic

XOR2 Simulation



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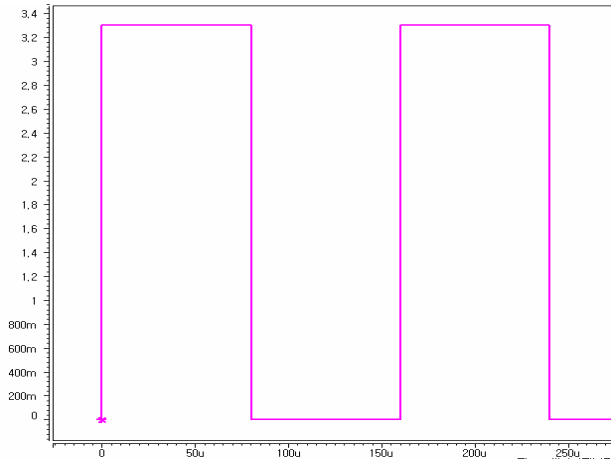

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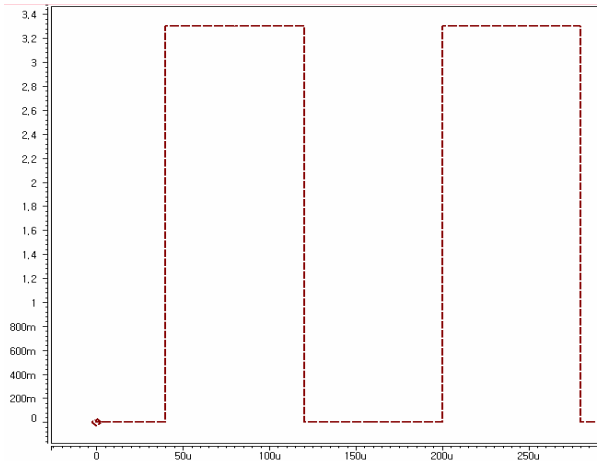
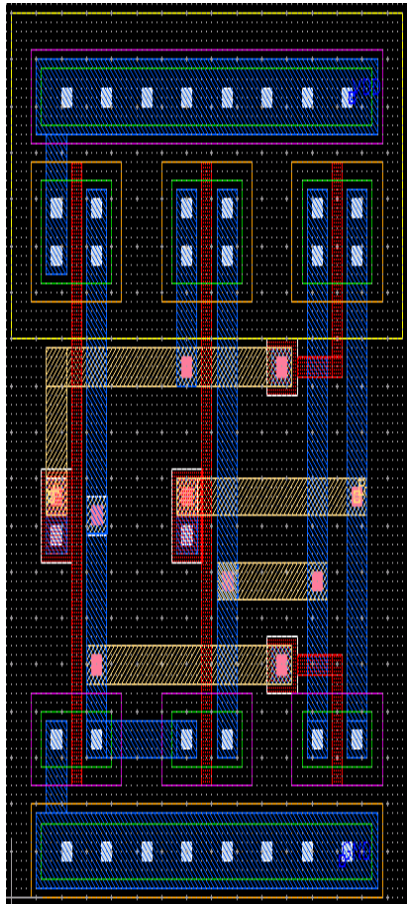
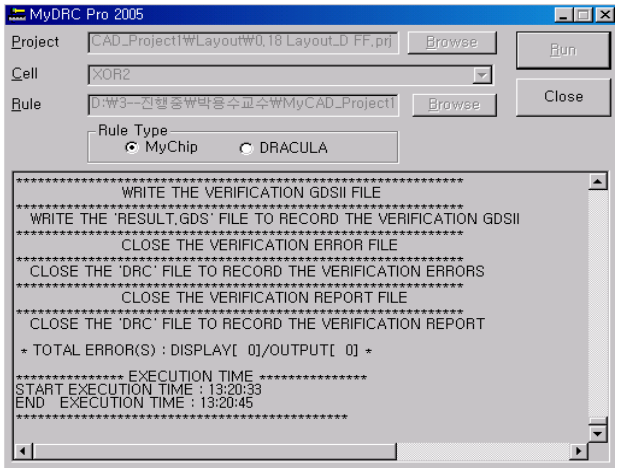


OUT

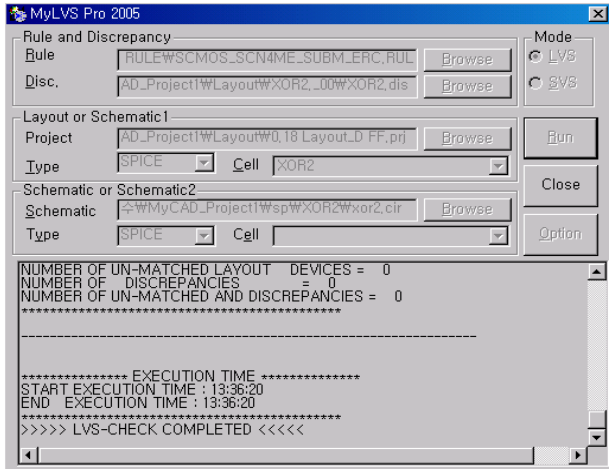
XOR2 layout and results of verification



Layout

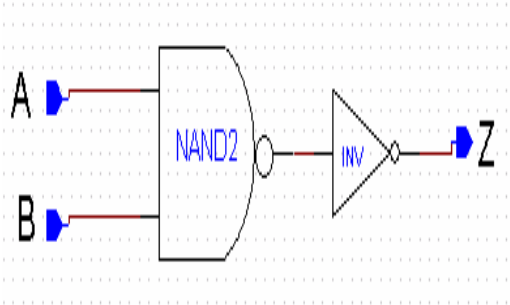


DRC result



LVS result

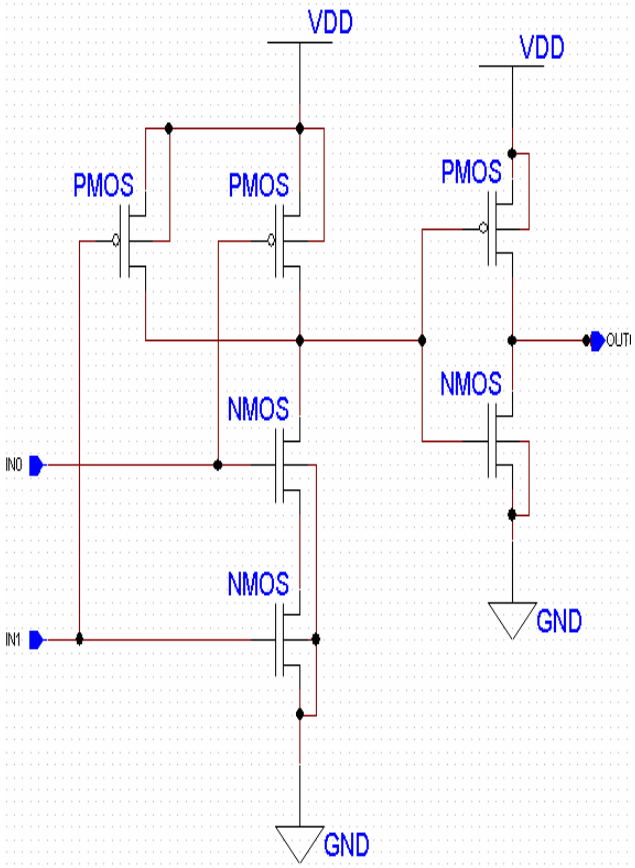
AND2 gate schematic and symbol



Logic Symbol

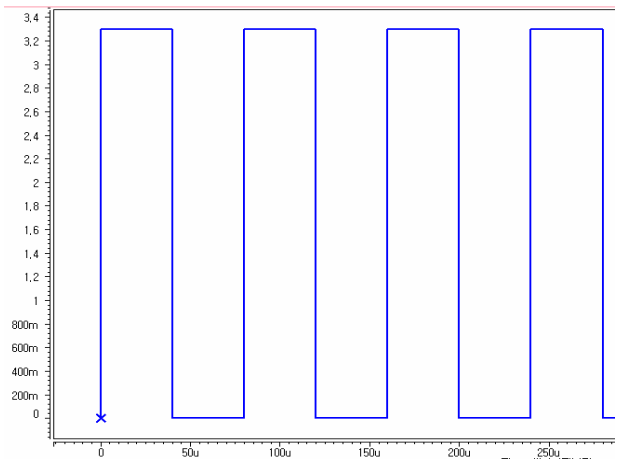
Input		Output
A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1

Truth Table



Schematic

AND2 Simulation



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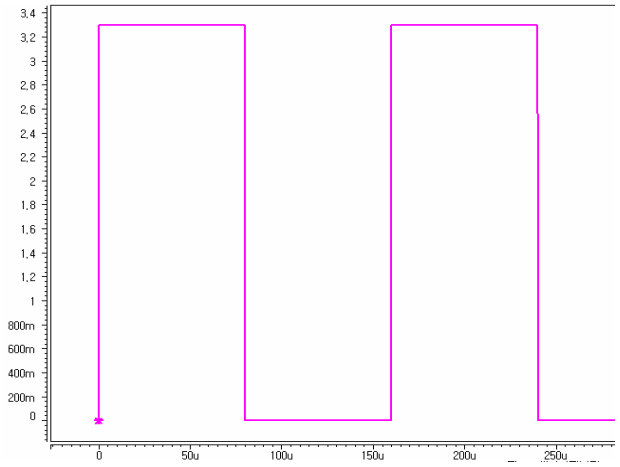
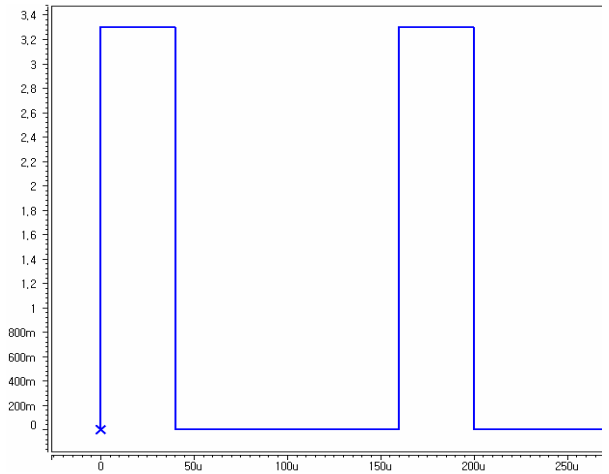
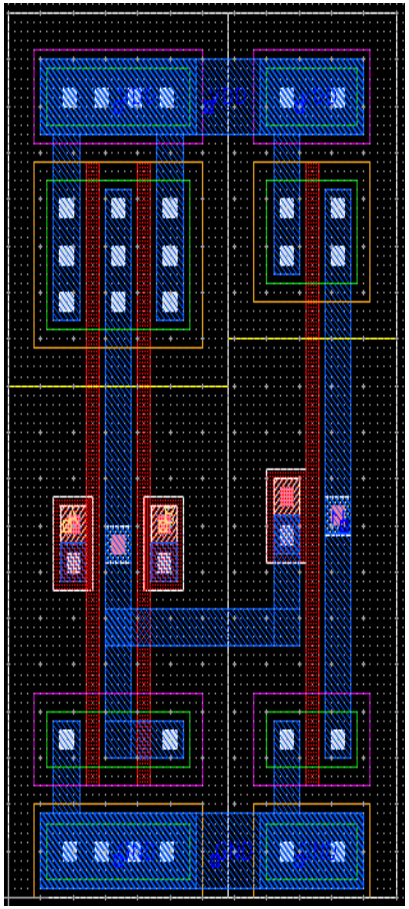


B

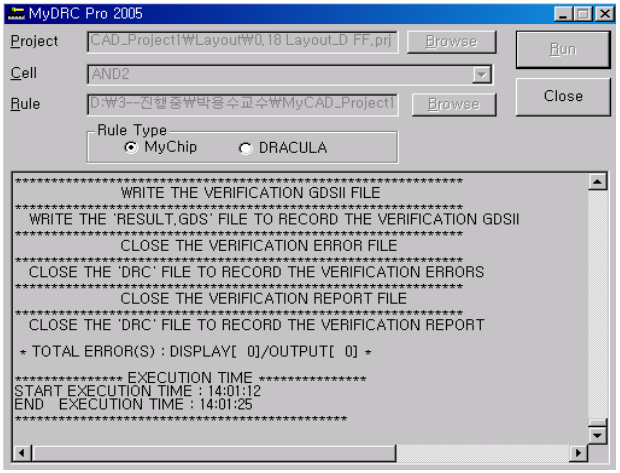


Z

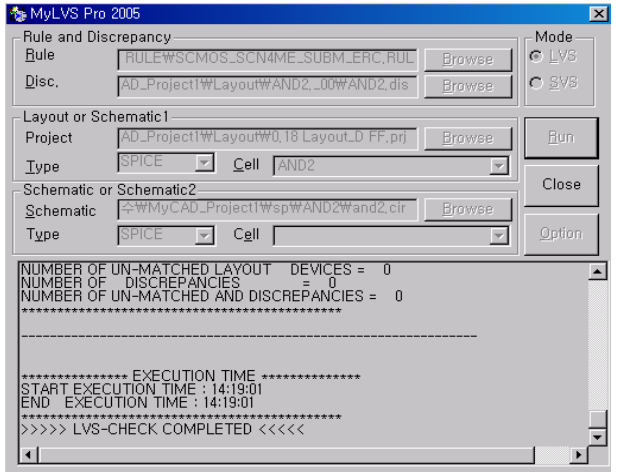
AND2 layout and results of verification



Layout

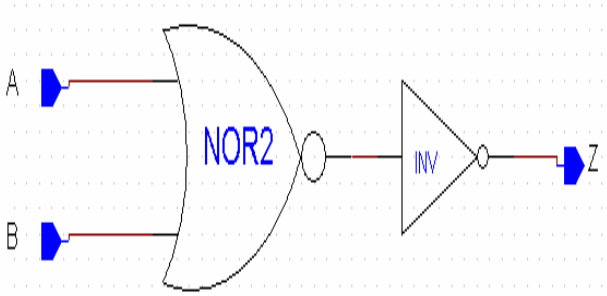


DRC result



LVS result

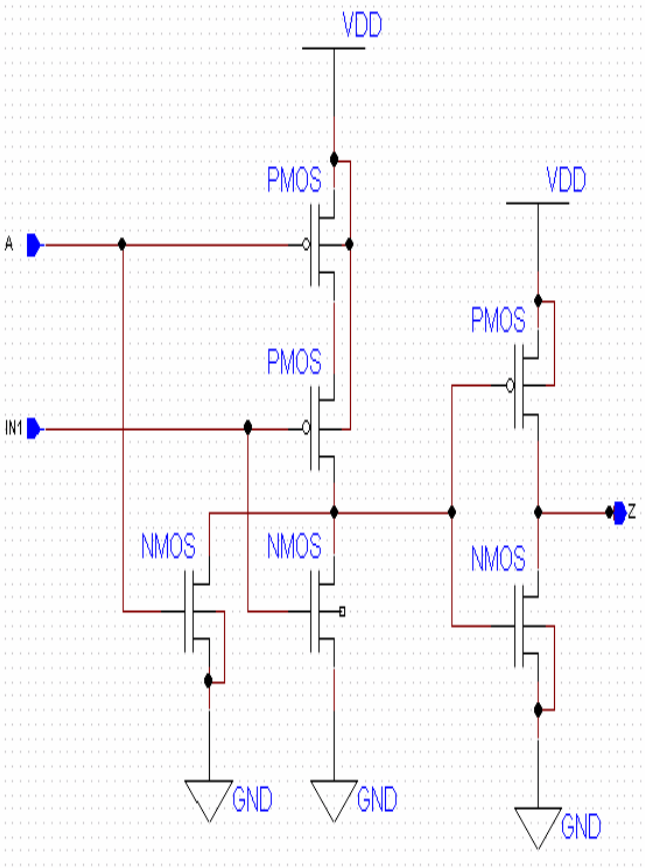
OR2 gate schematic and symbol



Logic Symbol

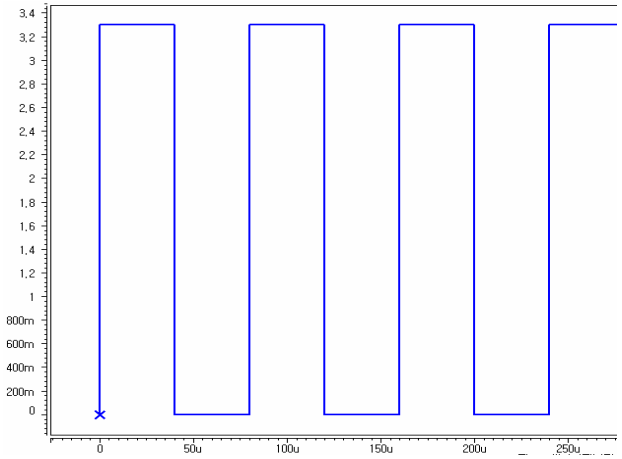
Input		Output
A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

Truth Table

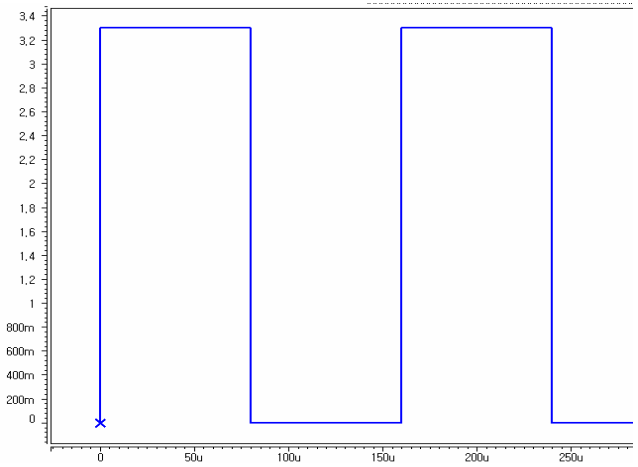


Schematic

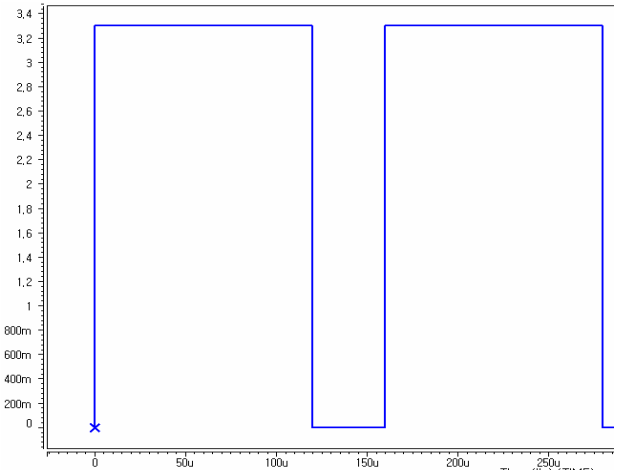
OR2 Simulation



A

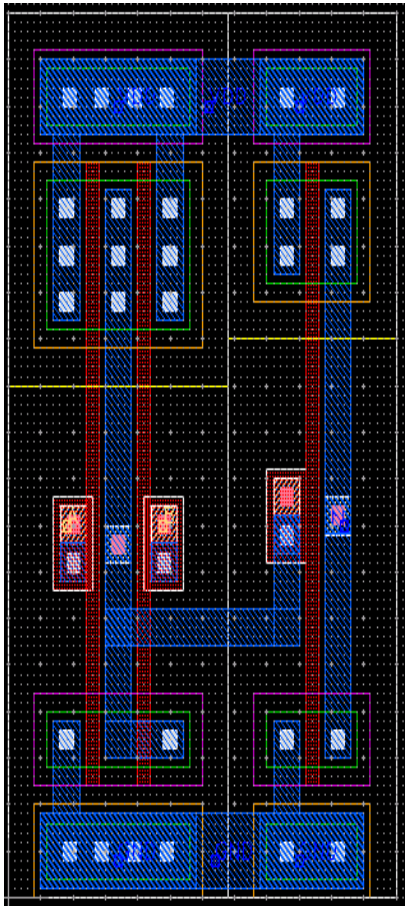


B

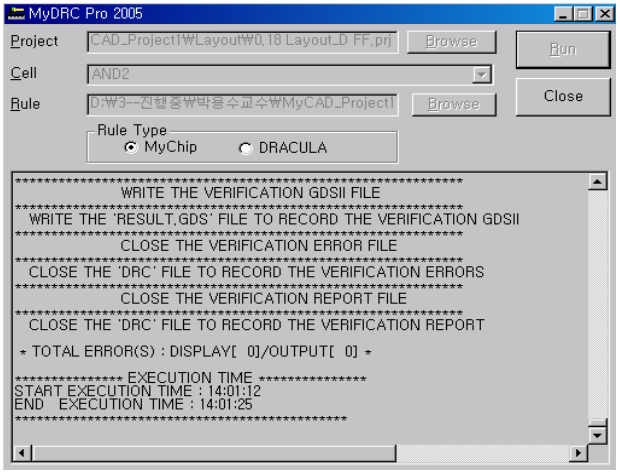


Z

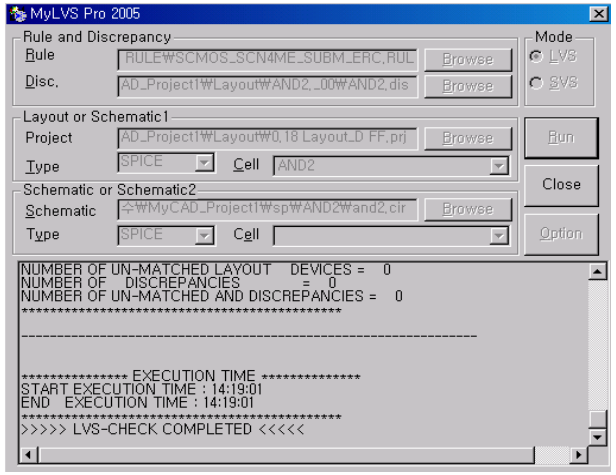
OR2 layout and results of verification



Layout



DRC result



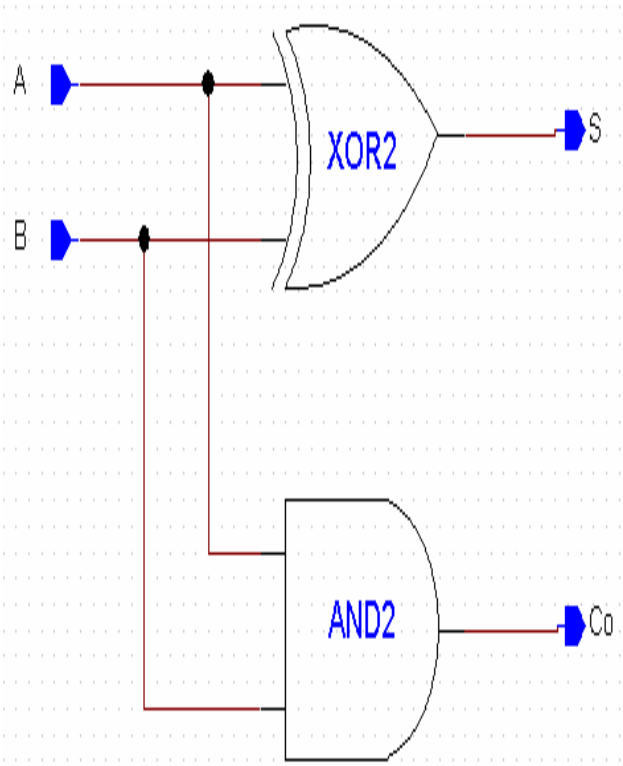
LVS result

HA schematic and symbol

Logic Symbol

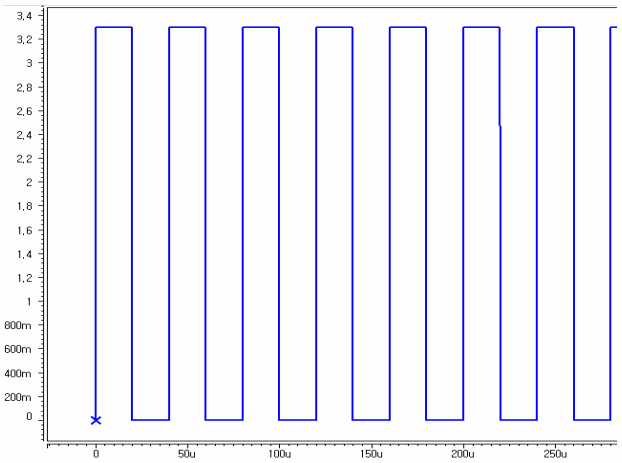
A	B	S	C0
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table

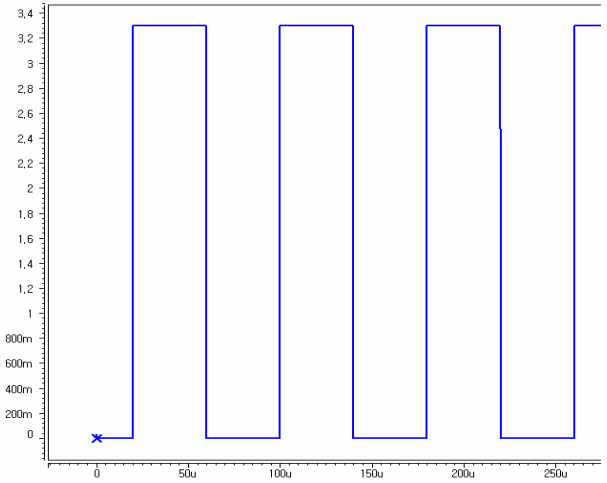


Schematic

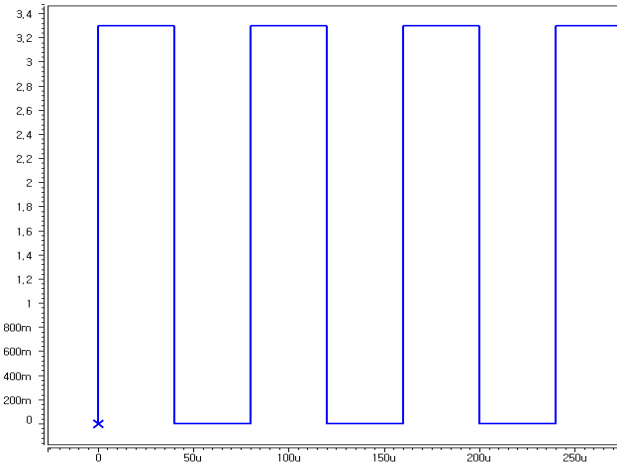
HA Simulation



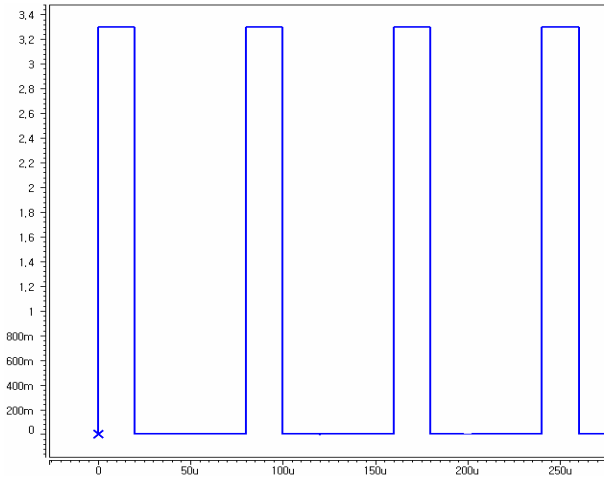
A



OUT

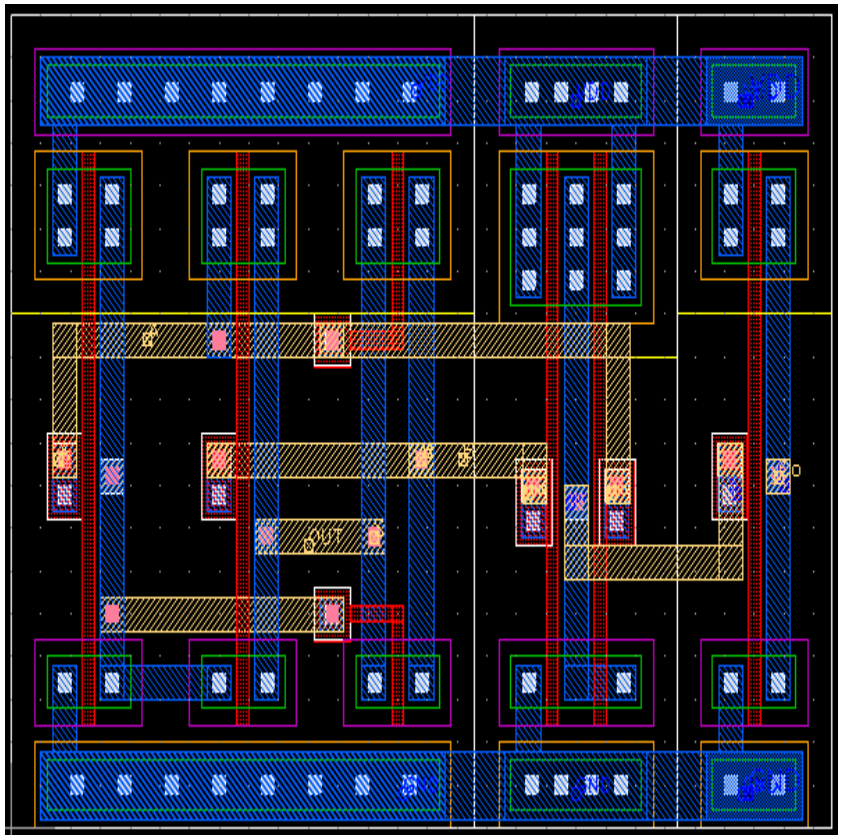


B

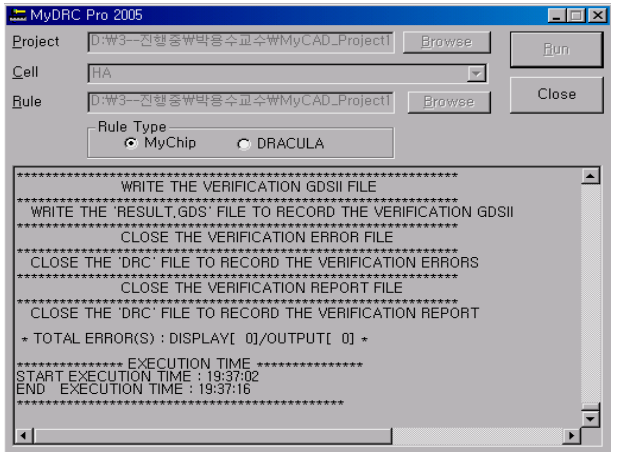


Co

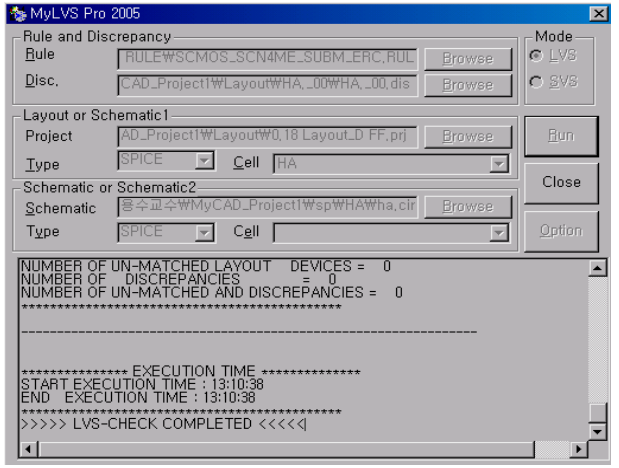
HA layout and results of verification



Layout

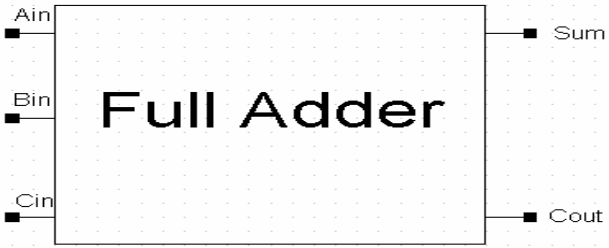


DRC result



LVS result

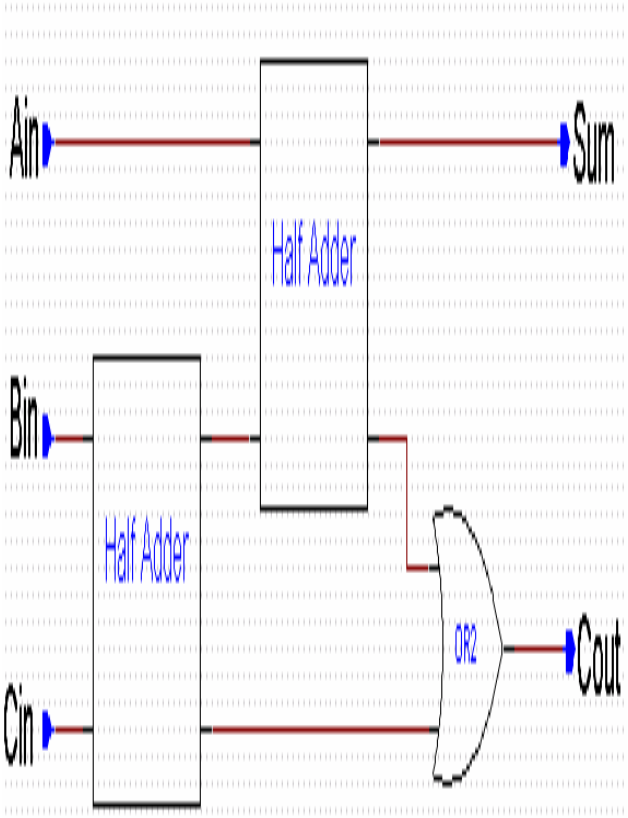
FA schematic and symbol



Logic Symbol

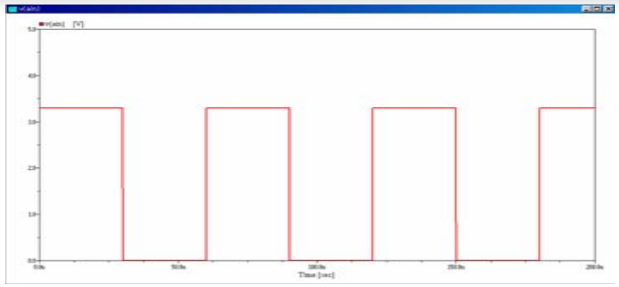
Input			Output	
Ain	Bin	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table

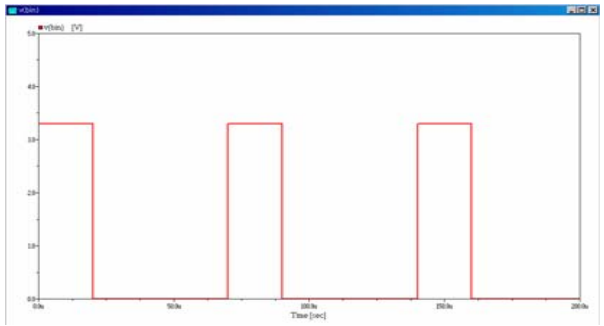


Schematic

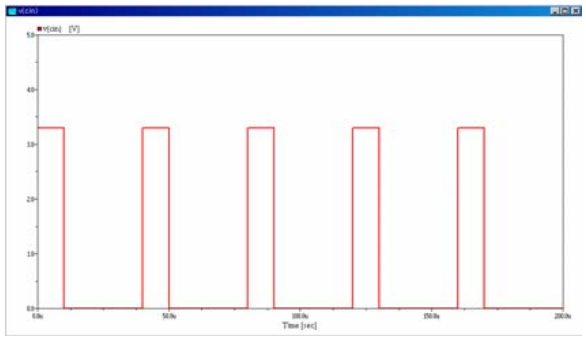
FA Flip-Flop Simulation



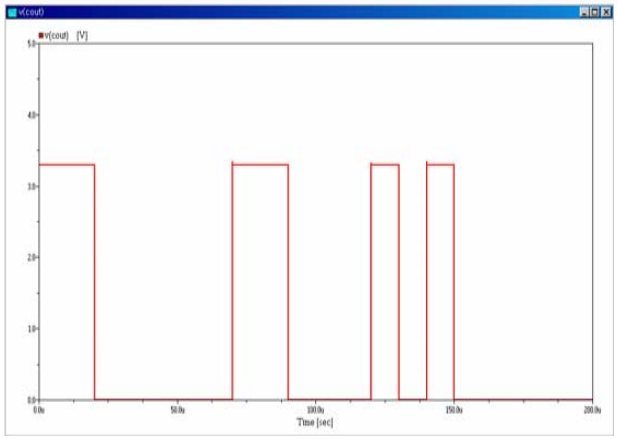
Ain



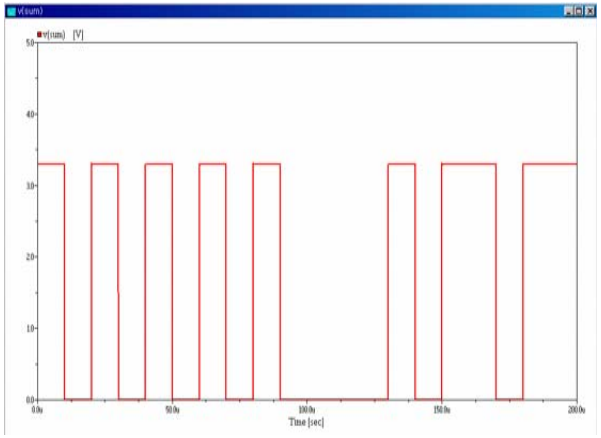
Bin



Cin

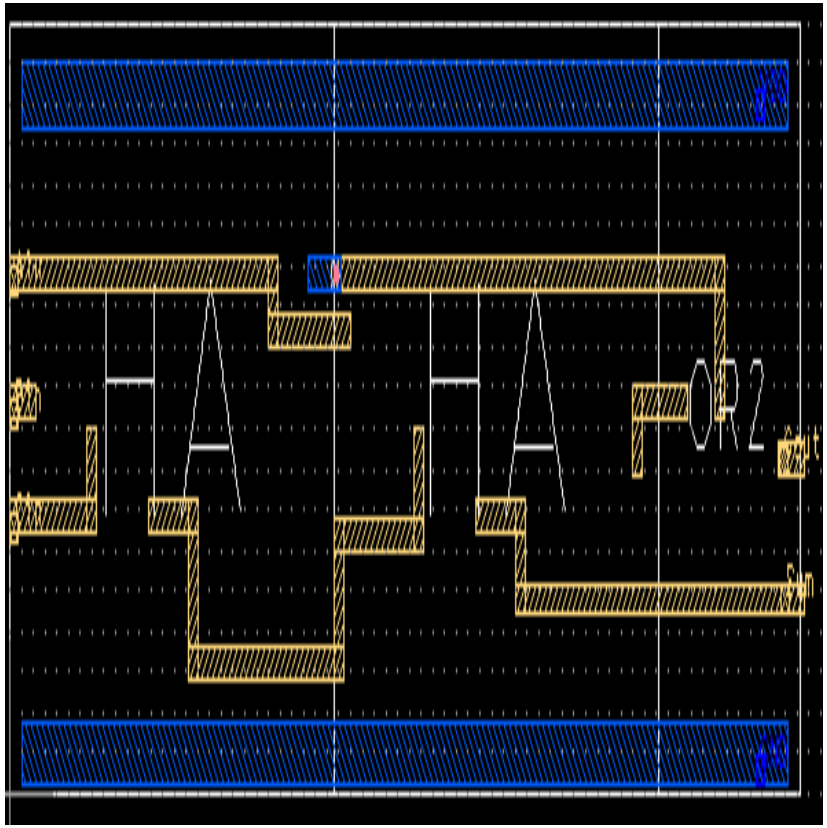


Cout

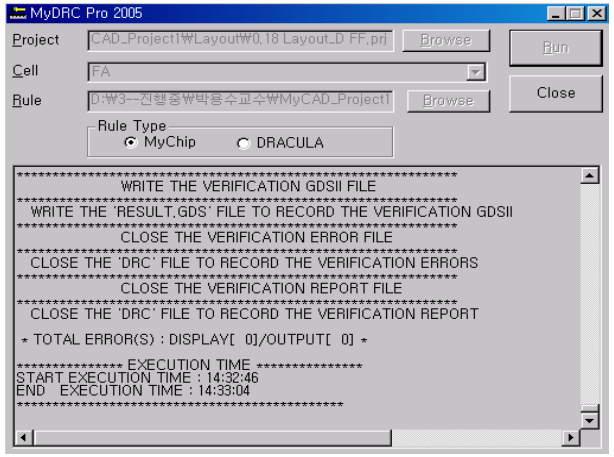


Q (output)

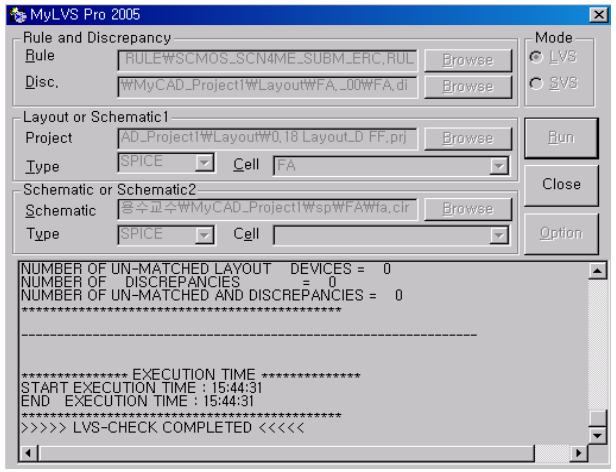
FA layout and results of verification



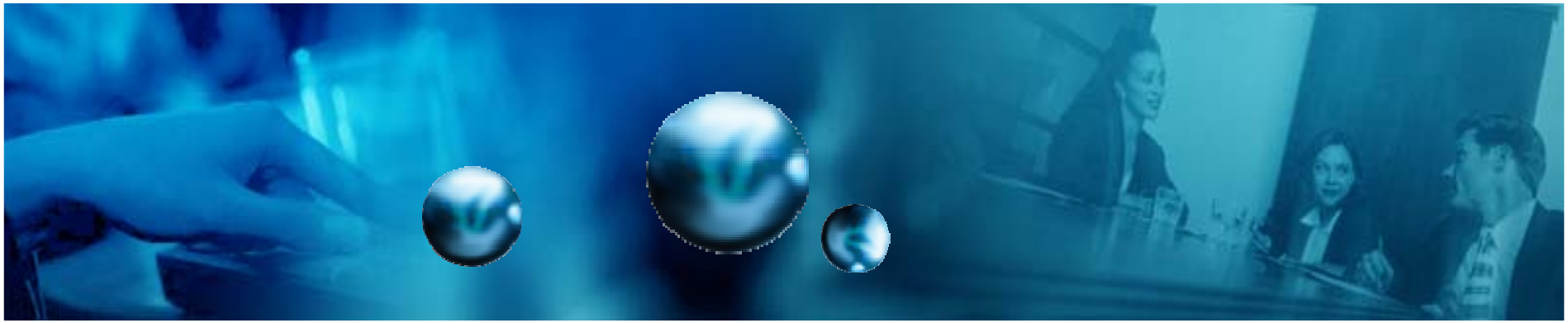
Layout



DRC result



LVS result



The End