



D Flip-Flop Design

Design Practice - MyCAD



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- This document provides the information on how to design D Filp-Flop schematic and layout.
- D Flip-Flop is designed based on MOSIS SCMOS layout rules.
- If you want to get more information, please refer to the related documents as below.
 - MyCAD Tutorial :
 - Learn how to use schematic and layout editor.
 - MySpice Tutorial :
 - Learn about simulating a circuit.
 - MyChip Pro Verification Reference Manual : Look up specific verification commands.

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Logic Symbol

| Input | Output | |
|-------|--------|--|
| IN | OUT | |
| 0 | 1 | |
| 1 | 0 | |





Inverter Simulation





Inverter layout and results of verification







| Rule and Dis Rule | Crepancy CMCS_SCN6M_SUBM_ERC(0,18um),rul Browse | |
|--------------------------------------|---|-------|
| <u>D</u> isc. | Browse | |
| Layout or Sc | hematic1 | |
| Project | /CAD_Project#Layout#0,18 Layout_D FF.prj Browse | Bun |
| <u>Т</u> уре | SPICE <u>Cell</u> Inverter | |
| Schematic o | r Schematic2 | Close |
| <u>S</u> chematic | C:#MyCAD_Project#Inverter#inverter.spc Browse | |
| Т⊻ре | SPICE Cell | |
| NUMBER OF NUMBER OF NUMBER OF | UN-MATCHEDLAYOUT DEVICES = 0 DISCREPANCIES = 0 UN-MATCHED AND DISCREPANCIES = 0 | |
| | | |
| *********** | THE CAL THE PE & 10,07,10 | |
| START EXEC | UTION TIME : 13:07:48 UTION TIME : 13:07:48 | |
| START EXE(END EXEC >>>>> LVS- | CUTION TIME : 13:07:48 UTION TIME : 13:07:48 CHECK COMPLETED <<<<< | |







Logic Symbol

| INO | IN1 | OUT |
|-----|-----|-----|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Truth Table





NAND2 Simulation







NAND2 layout and results of verification















Logic Symbol

| Input | | | Output |
|-------|---|---|--------|
| А | В | С | OUT |
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |







NAND3 layout and results of verification







NUMBER OF UN-MATCHED LAYOUT DEVICES = 0 NUMBER OF DISCREPANCIES = 0 NUMBER OF UN-MATCHED AND DISCREPANCIES = 0

START EXECUTION TIME ** START EXECUTION TIME : 18:15:34 END EXECUTION TIME : 18:15:34

>>>>> LVS-CHECK COMPLETED <<<<<

LVS result

D Flip-Flop schematic and symbol





Logic Symbol

| Input | | Output | |
|-------|---|--------|-------|
| CLK | D | Q | Q_bar |
| Ţ | 0 | 0 | 1 |
| Ŷ | 1 | 1 | 0 |



Truth Table



D Flip-Flop Simulation







Clock

D (input)



D Flip-Flop layout and results of verification MyCAU^{**}



D Flip-Flop with Preset and Clear schematic and symbol





| INPUT | | OUTPUT | | | |
|-------|-----|--------|---|--------|------------|
| CLK | CLR | PRE | D | Q(t+1) | Q_bar(t+1) |
| Х | 0 | 1 | Х | 0 | 1 |
| Х | 1 | 0 | Х | 1 | 0 |
| Х | 0 | 0 | Х | 1 | 1 |
| 1 | 1 | 1 | Х | Q(t) | Q_bar(t) |
| 0 | 1 | 1 | Х | Q(t) | Q_bar(t) |
| 1 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

Truth Table



Schematic

D Flip-Flop with Preset and Clear Simulation (1/2)





D Flip-Flop with Preset and Clear Simulation (2/2)





D Flip-Flop with Preset and Clear layout and results of verification









The End