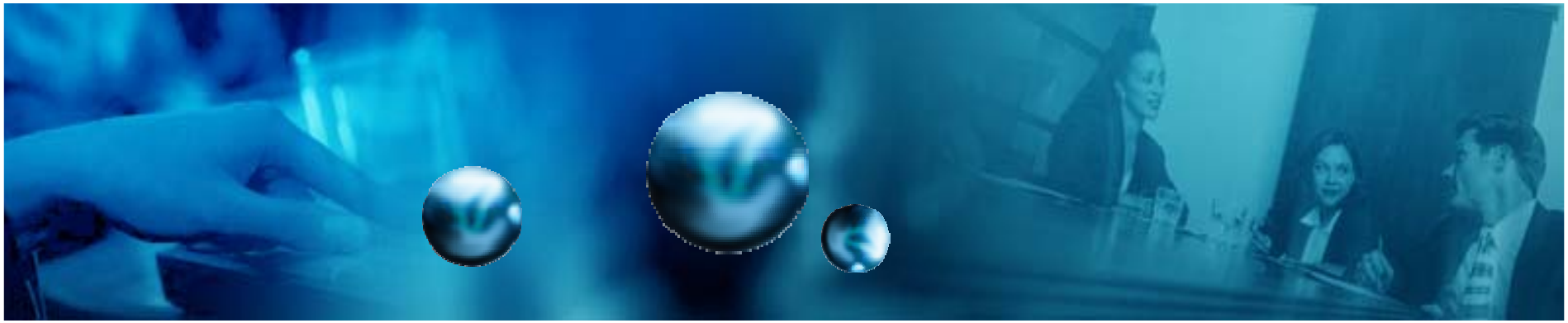


D Flip-Flop Design

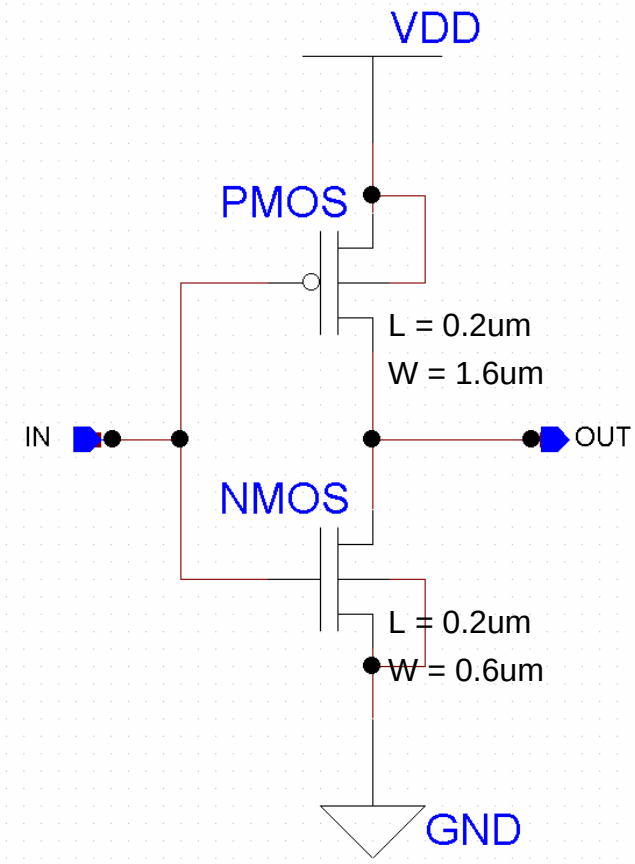
Design Practice - MyCAD

Table of Contents

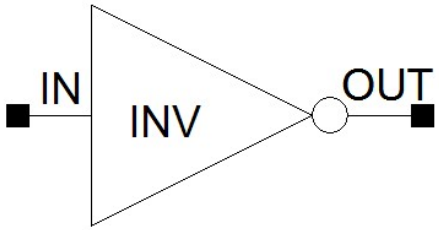
Preface

- This document provides the information on how to design D Filp-Flop schematic and layout.
- D Flip-Flop is designed based on MOSIS SCMOS layout rules.
- If you want to get more information, please refer to the related documents as below.
  - MyCAD Tutorial :
    Learn how to use schematic and layout editor.
  - MySpice Tutorial :
    Learn about simulating a circuit.
  - MyChip Pro Verification Reference Manual :
    Look up specific verification commands.

Inverter schematic and symbol



Schematic

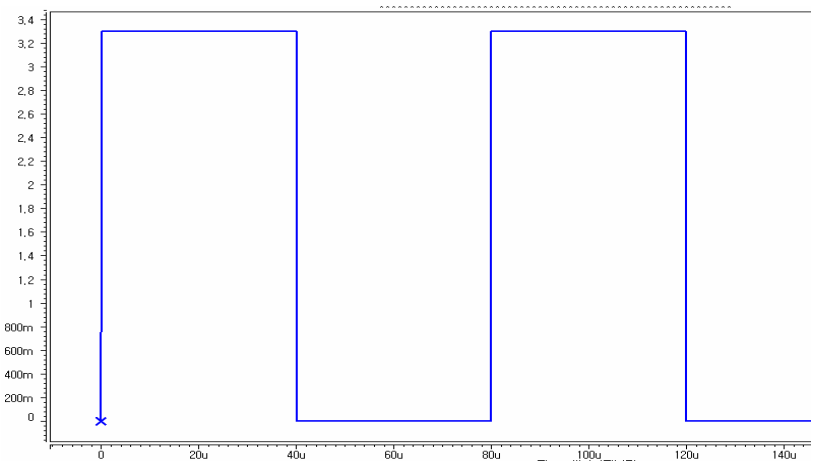


Logic Symbol

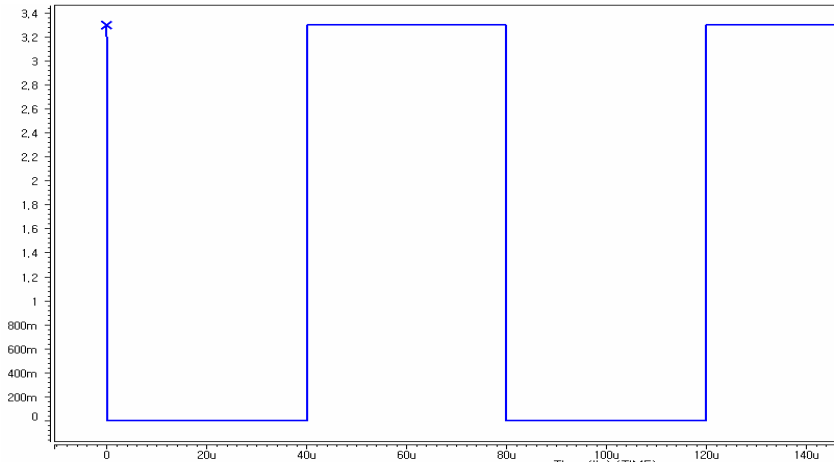
Input	Output
IN	OUT
0	1
1	0

Truth Table

Inverter Simulation

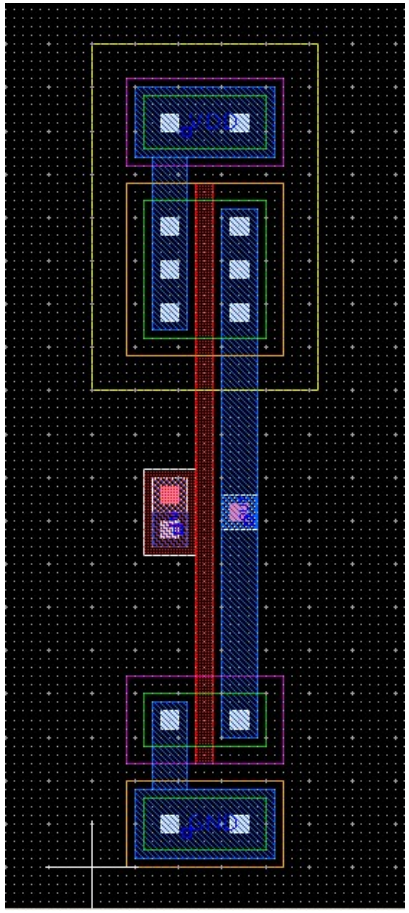


IN

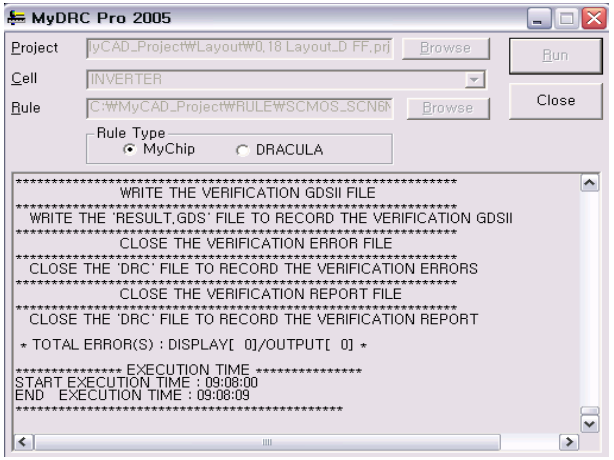


OUT

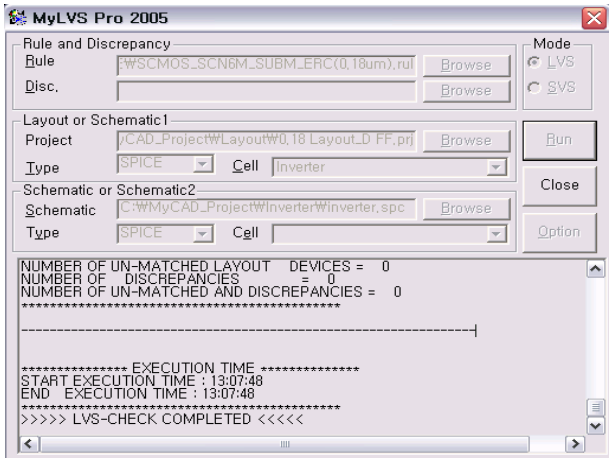
Inverter layout and results of verification



Layout

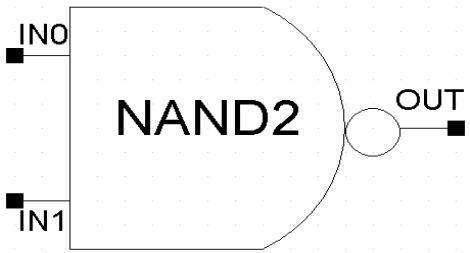


DRC result



LVS result

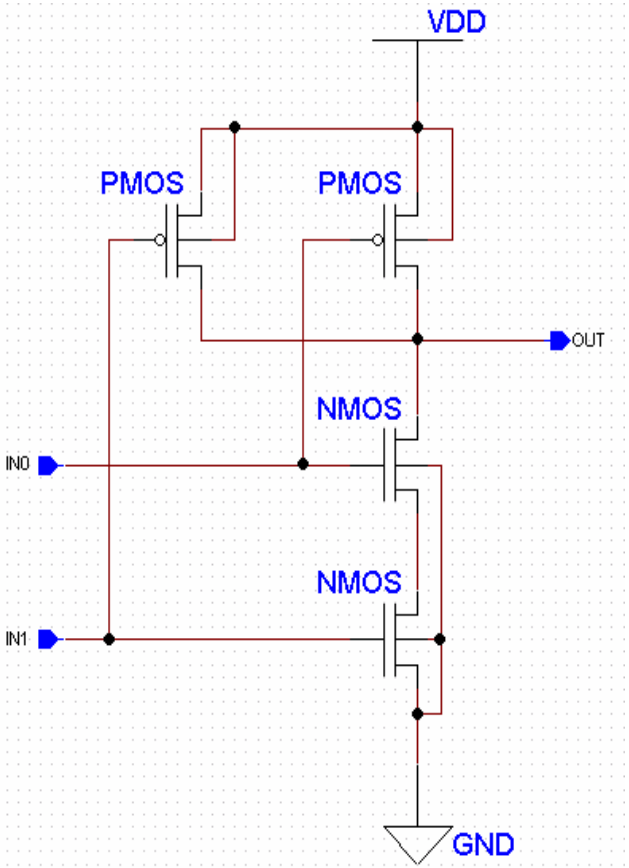
NAND2 schematic and symbol



Logic Symbol

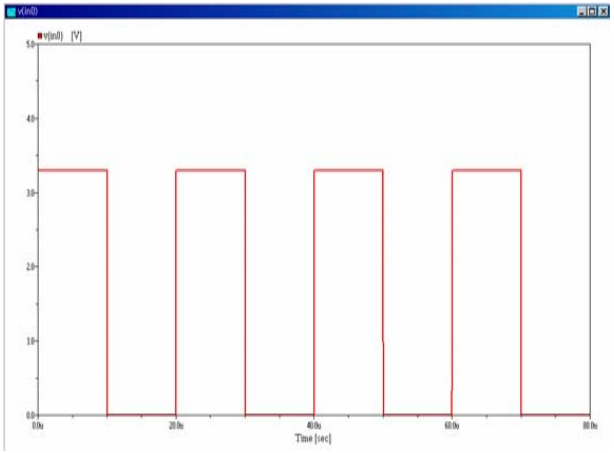
IN0	IN1	OUT
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table

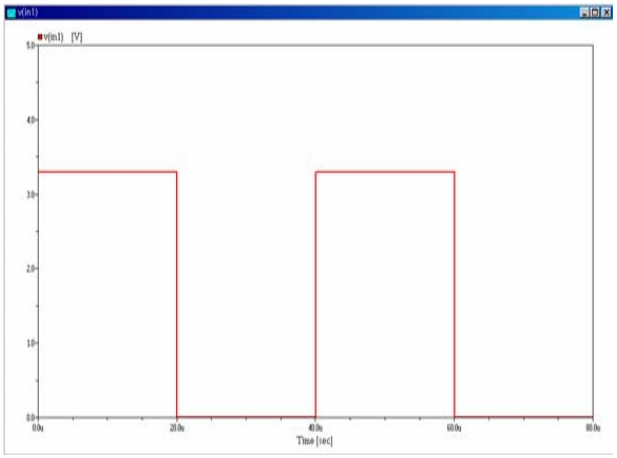


Schematic

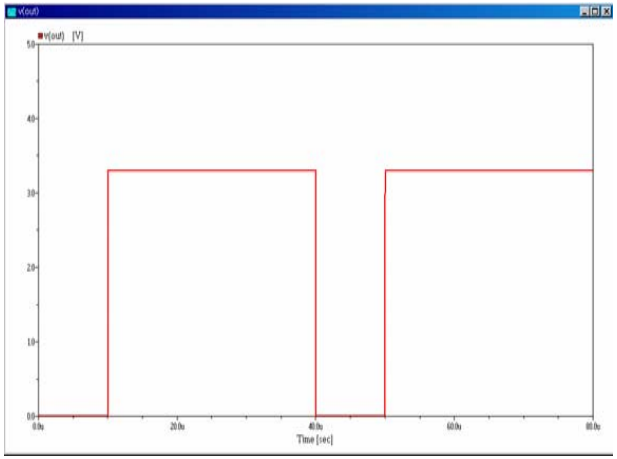
NAND2 Simulation



IN0

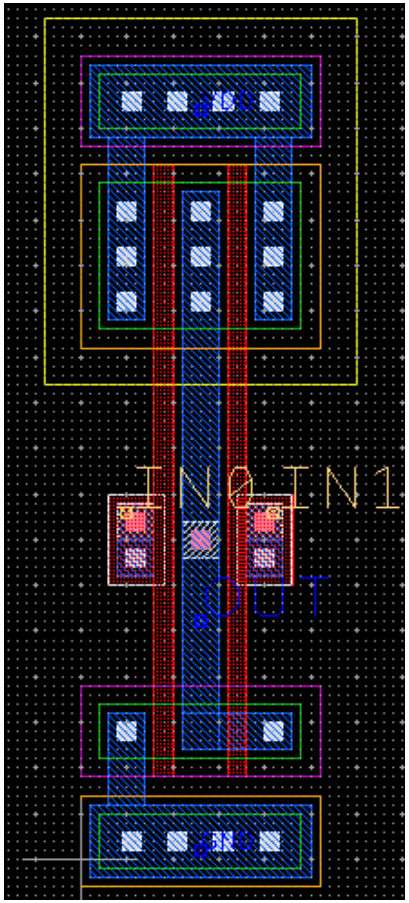


IN1

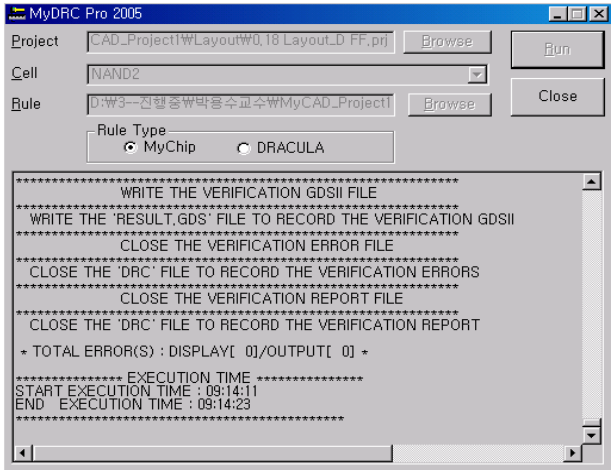


OUT

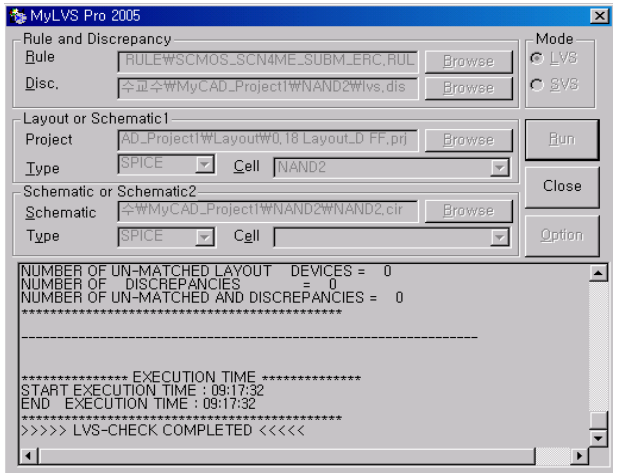
NAND2 layout and results of verification



Layout



DRC result



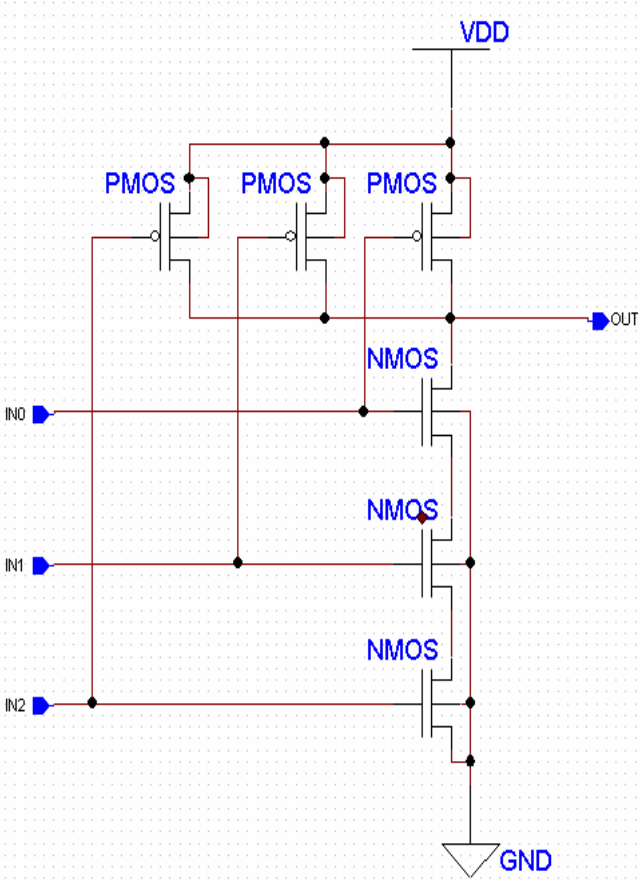
LVS result

NAND3 schematic and symbol

Logic Symbol

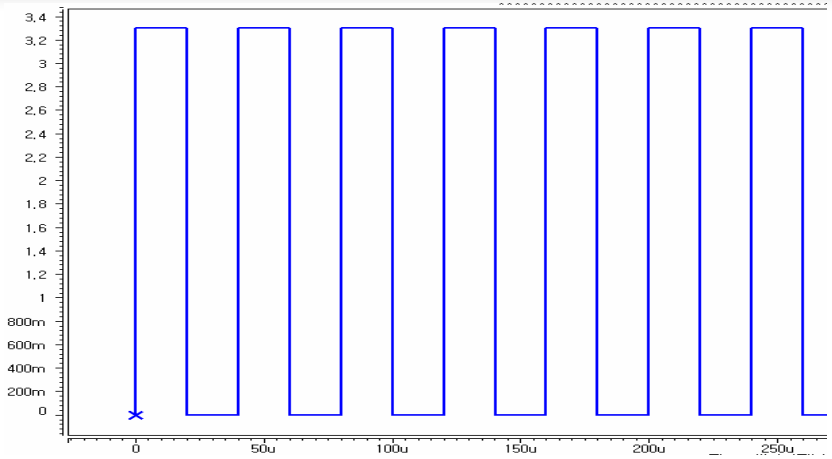
Input			Output
A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Truth Table

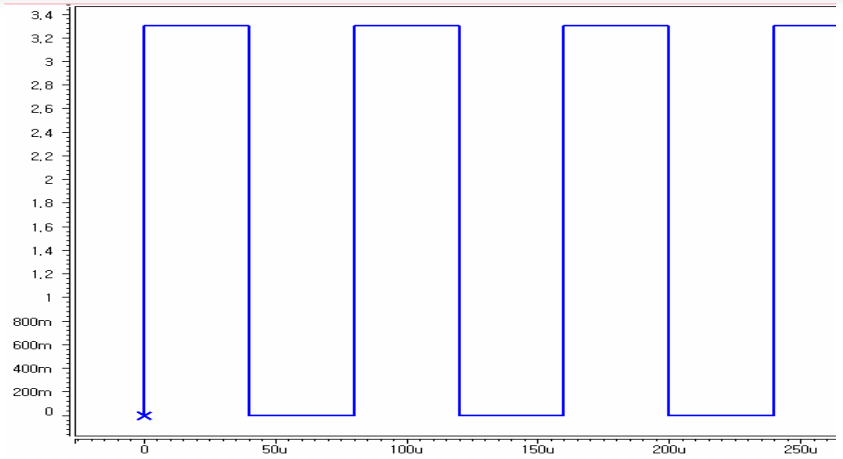


Schematic

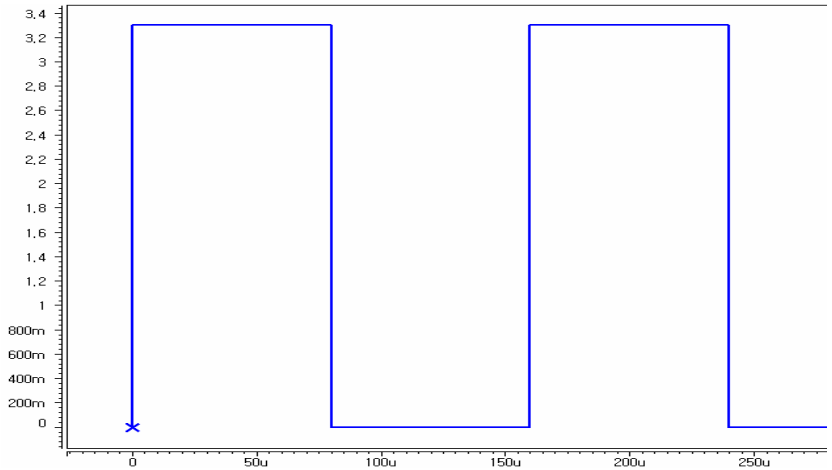
NAND3 Simulation



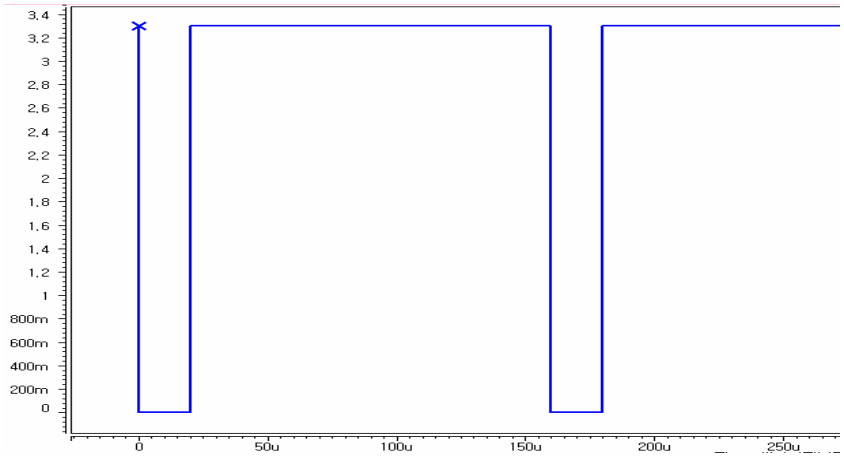
IN0



IN1

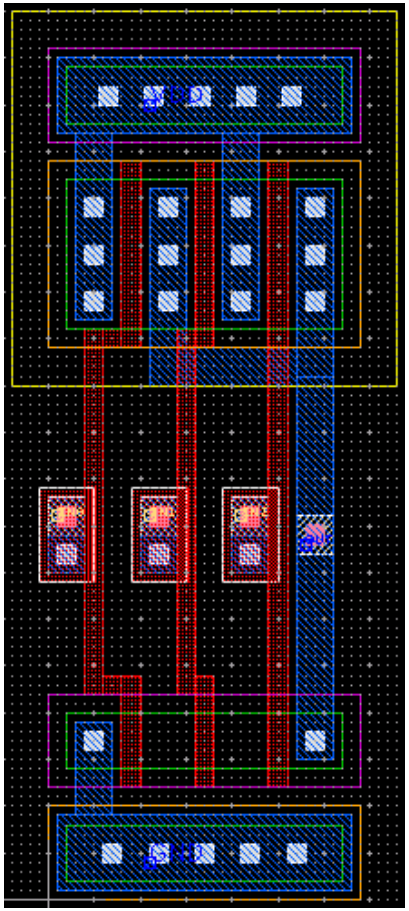


IN2

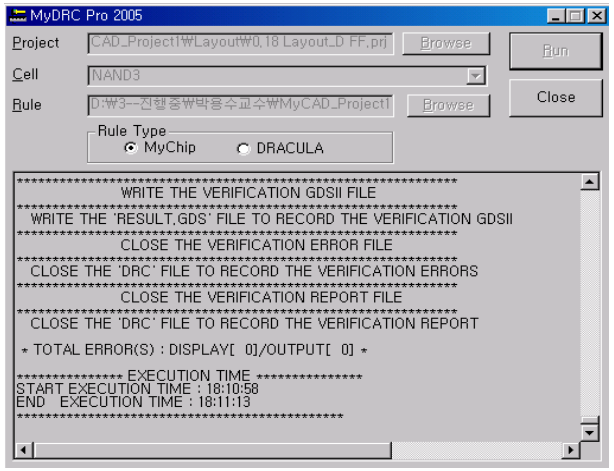


OUT

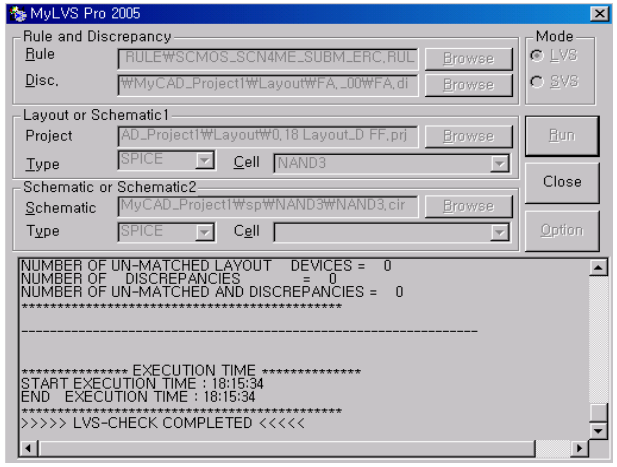
NAND3 layout and results of verification



Layout

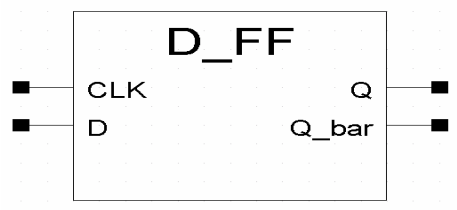


DRC result



LVS result

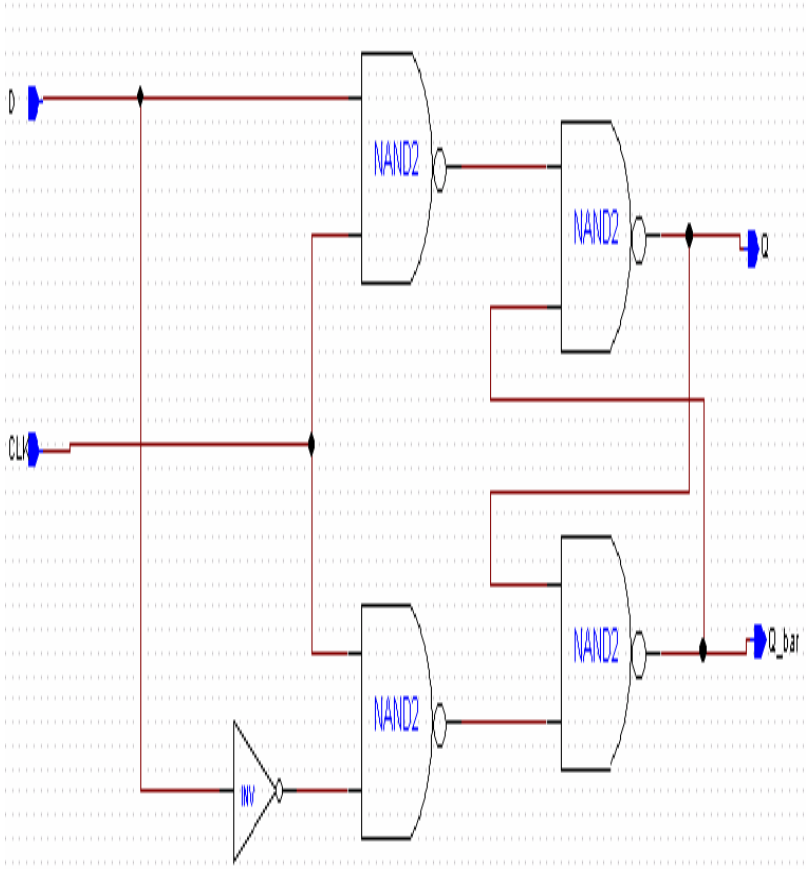
D Flip-Flop schematic and symbol



Logic Symbol

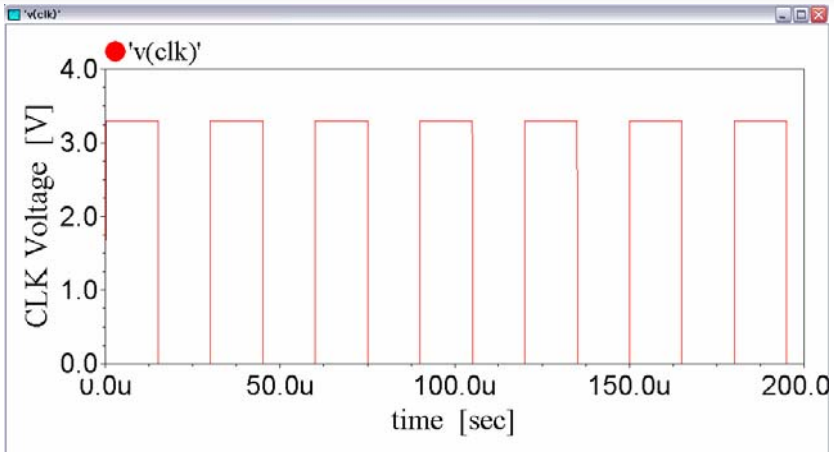
Input		Output	
CLK	D	Q	Q_bar
↑	0	0	1
↑	1	1	0

Truth Table

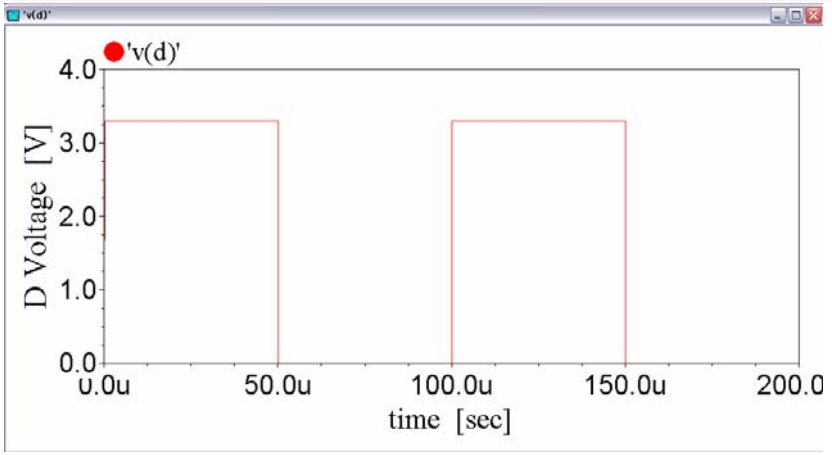


Schematic

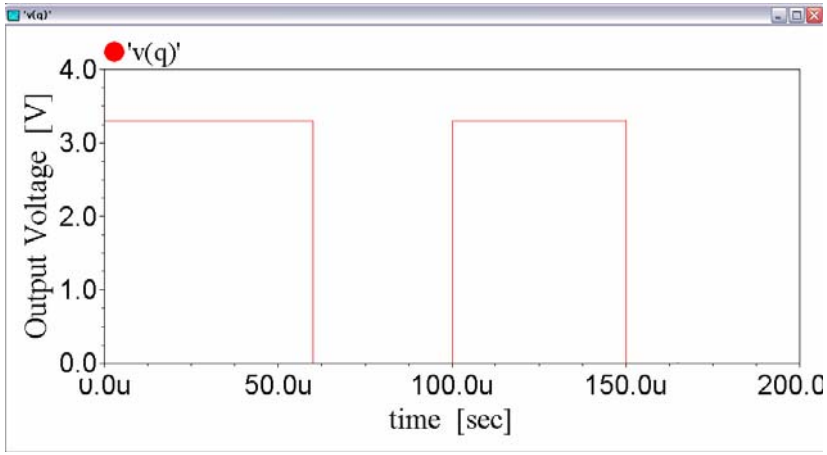
D Flip-Flop Simulation



Clock

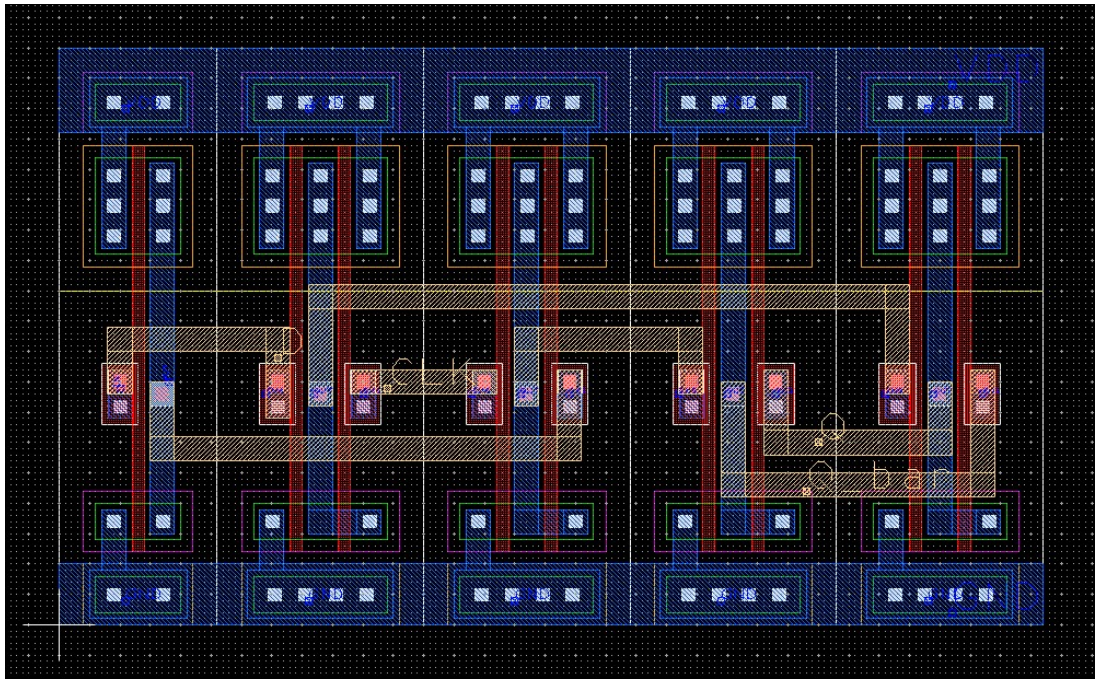


D (input)



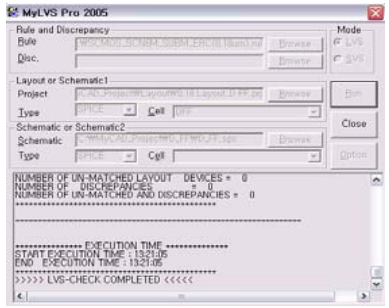
Q (output)

D Flip-Flop layout and results of verification



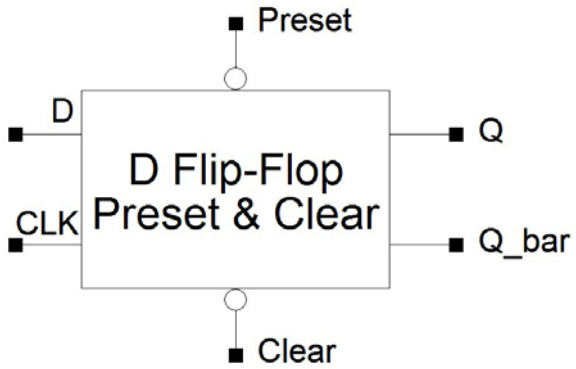
Layout

DRC result



LVS result

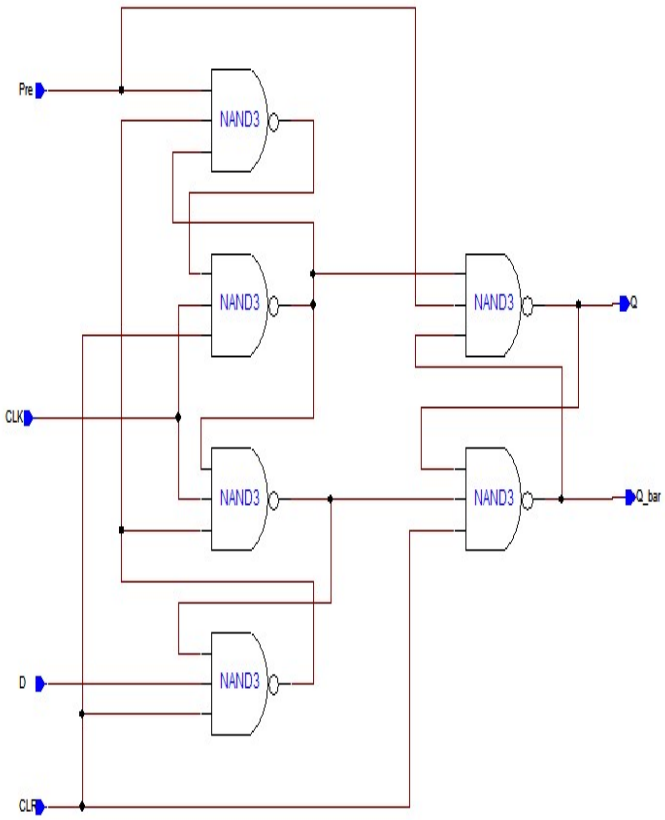
D Flip-Flop with Preset and Clear schematic and symbol



Logic Symbol

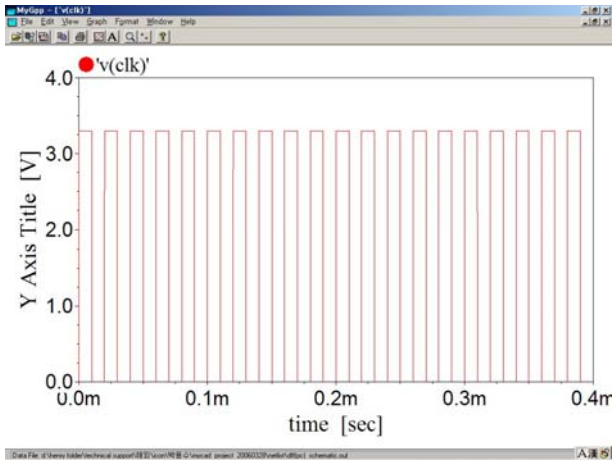
INPUT				OUTPUT	
CLK	CLR	PRE	D	Q(t+1)	Q_bar(t+1)
X	0	1	X	0	1
X	1	0	X	1	0
X	0	0	X	1	1
1	1	1	X	Q(t)	Q_bar(t)
0	1	1	X	Q(t)	Q_bar(t)
↑	1	1	0	0	1
↑	1	1	1	1	0

Truth Table

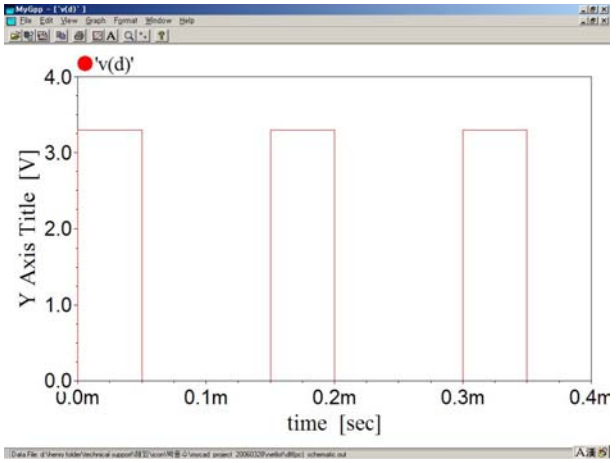


Schematic

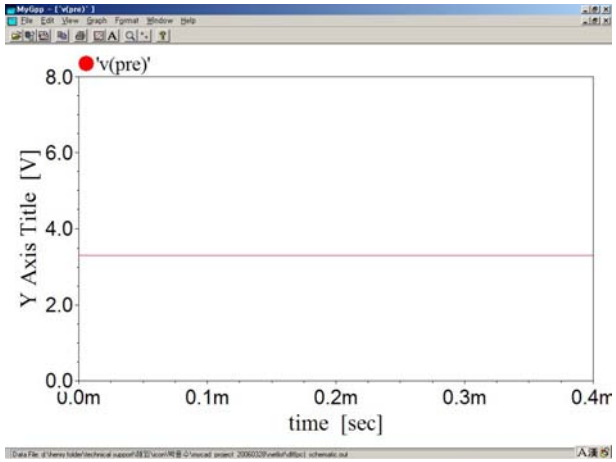
D Flip-Flop with Preset and Clear Simulation (1/2)



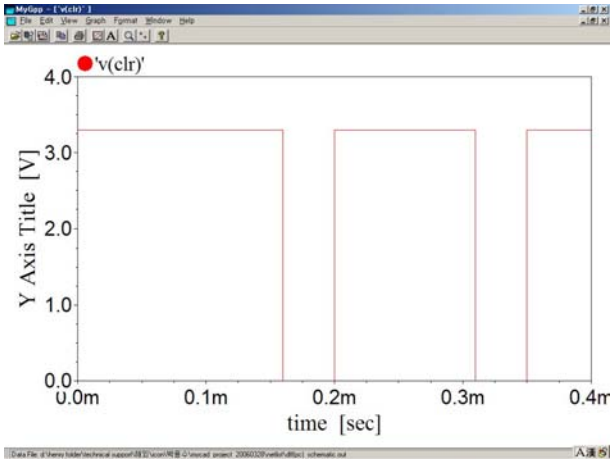
Clock



D (input)

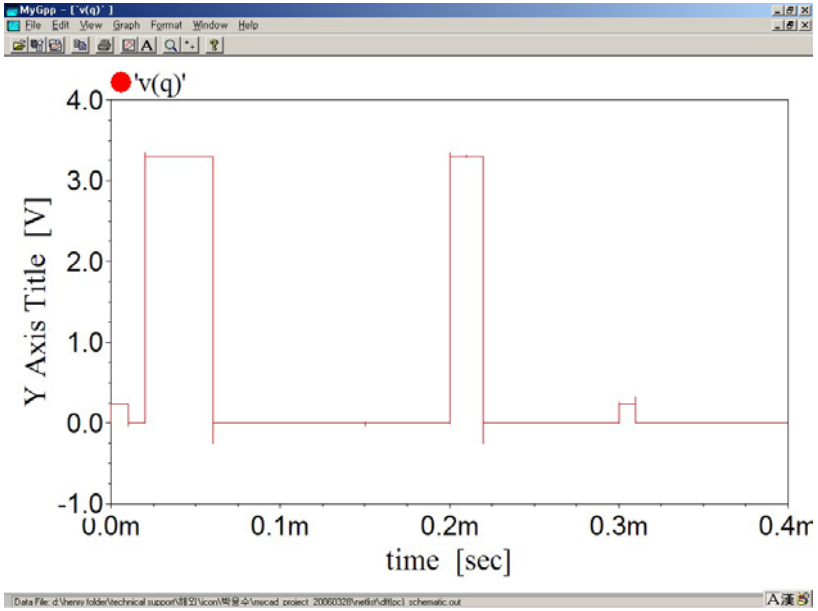


Preset

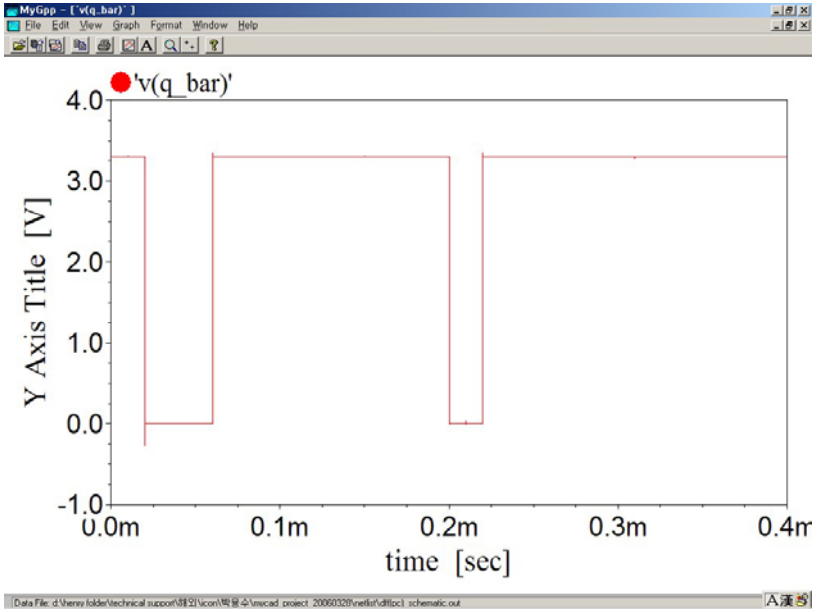


Clear

D Flip-Flop with Preset and Clear Simulation (2/2)

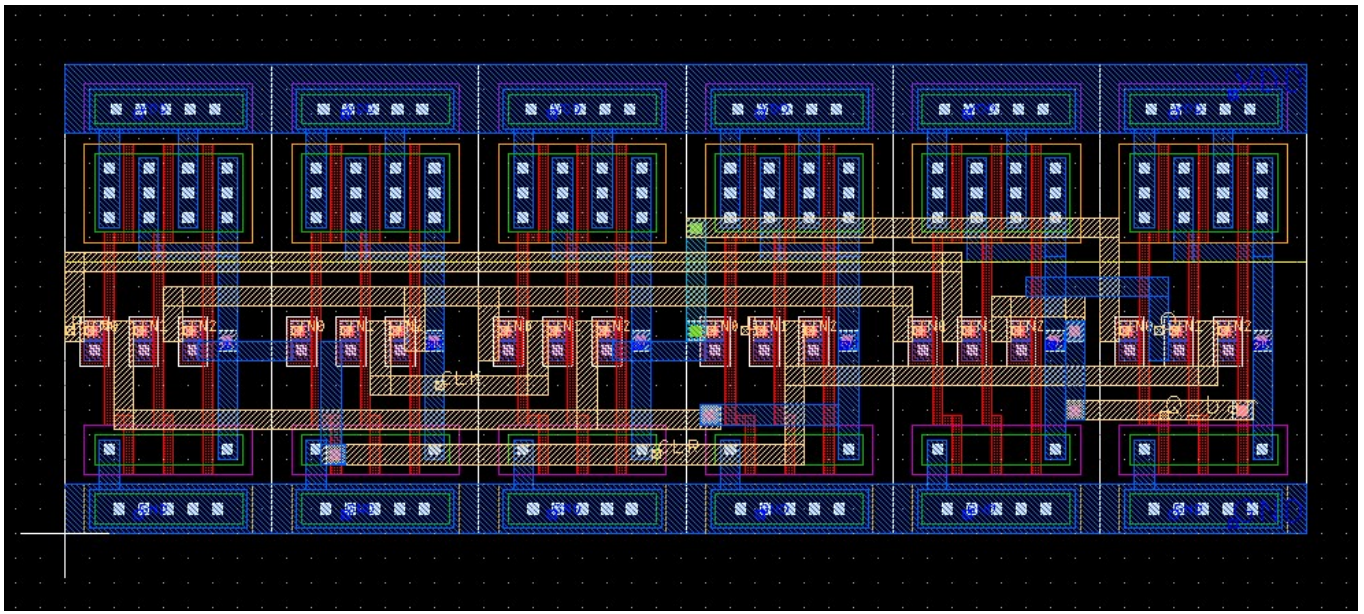


Q (output)

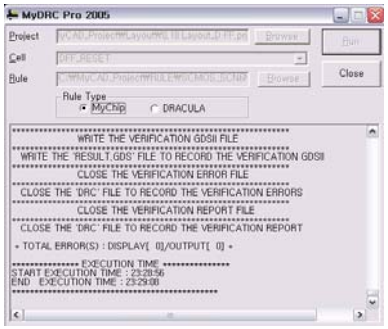


Q_bar (output)

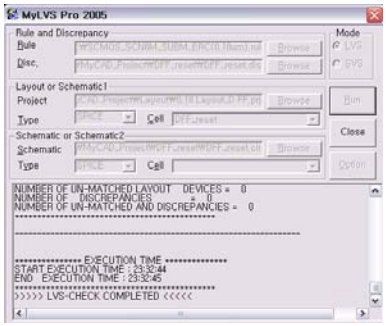
D Flip-Flop with Preset and Clear layout and results of verification



Layout

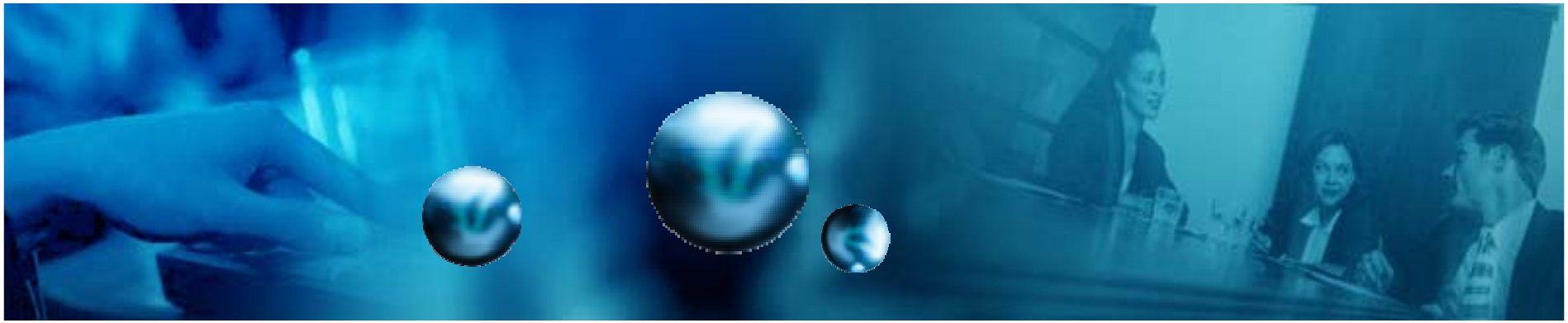


DRC result



LVS result

MyCAD™



The End